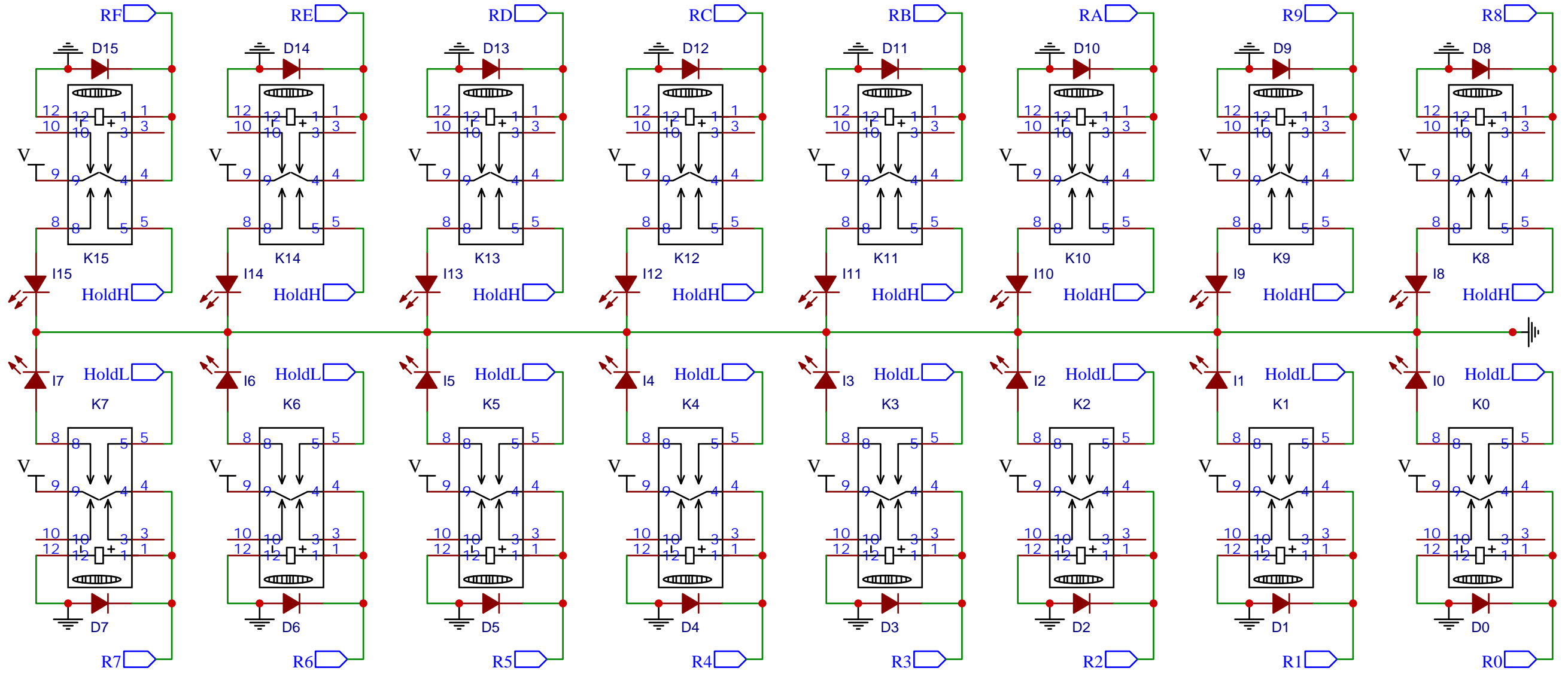
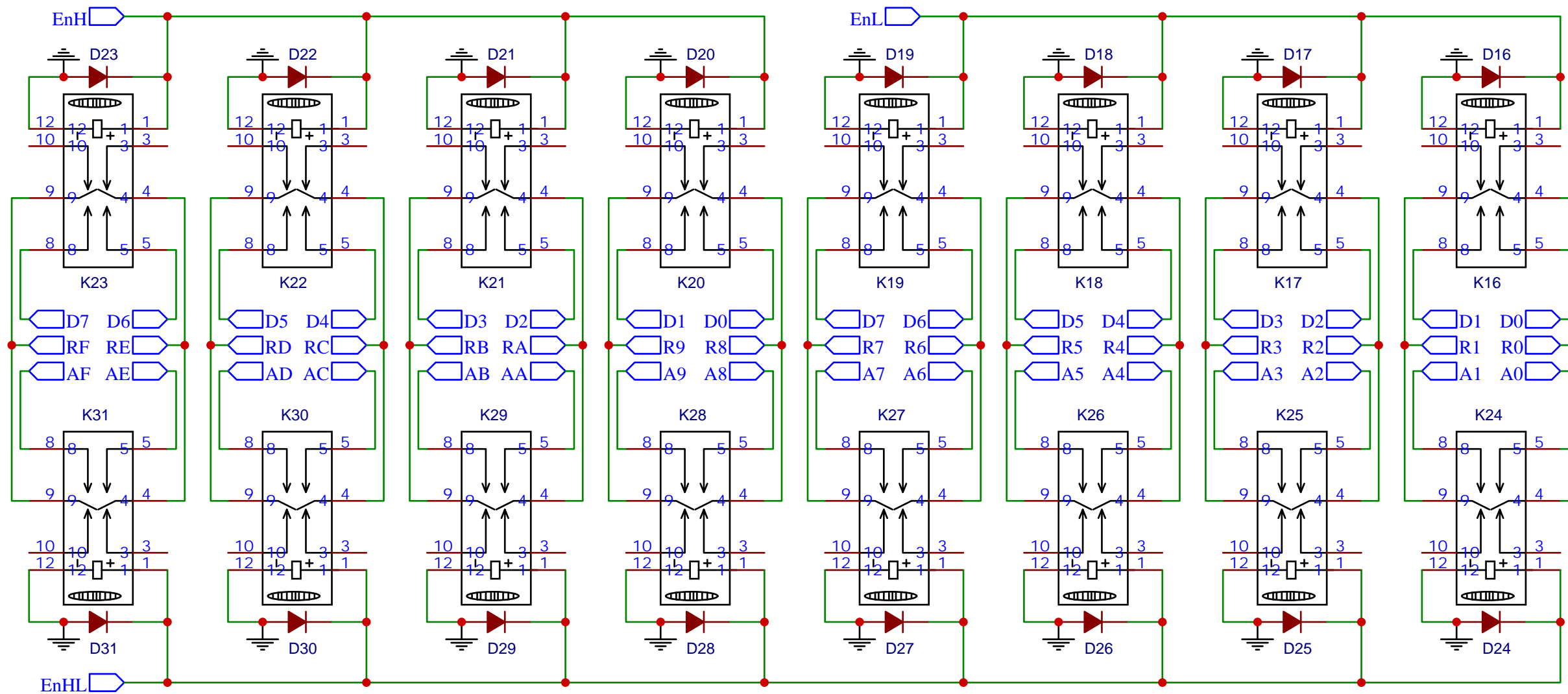


Sheet 1: 1-bit register stores (8-bit X + 8-bit Y)



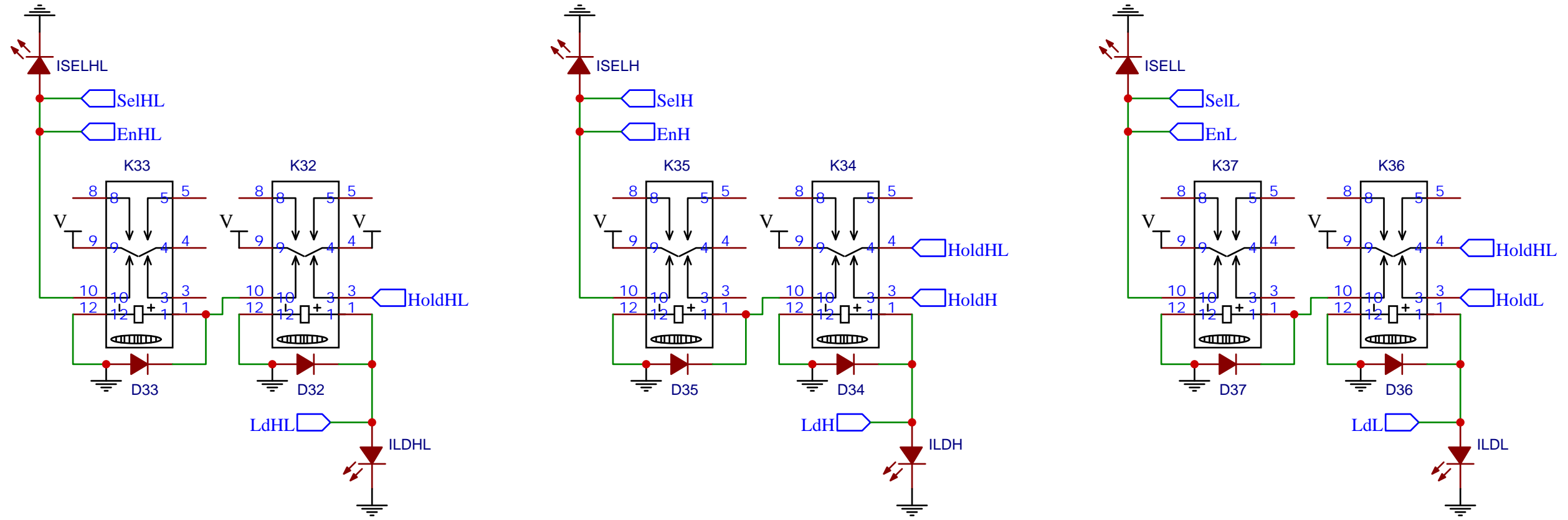
HoldH and HoldL signals connect to control relays (sheet 3)
 R0-RF signals connect to gating relays (sheet 2)

TITLE: Relay Computer : Y Backplane Registers		REV: 1.0
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EnX, ExY and EnXY signals connect to control relays (sheet 3)
 A0-AF signals connect to address bus (sheet 4)
 D0-D7 signals connect to data bus (sheet 4)
 R0-RF signals connect to register relays (sheet 1)

TITLE: Relay Computer : Y Backplane Registers		REV: 1.0
	Company: Paul Law	Sheet: 2/4
	Date: 2019-02-10	Drawn By: paul_6392

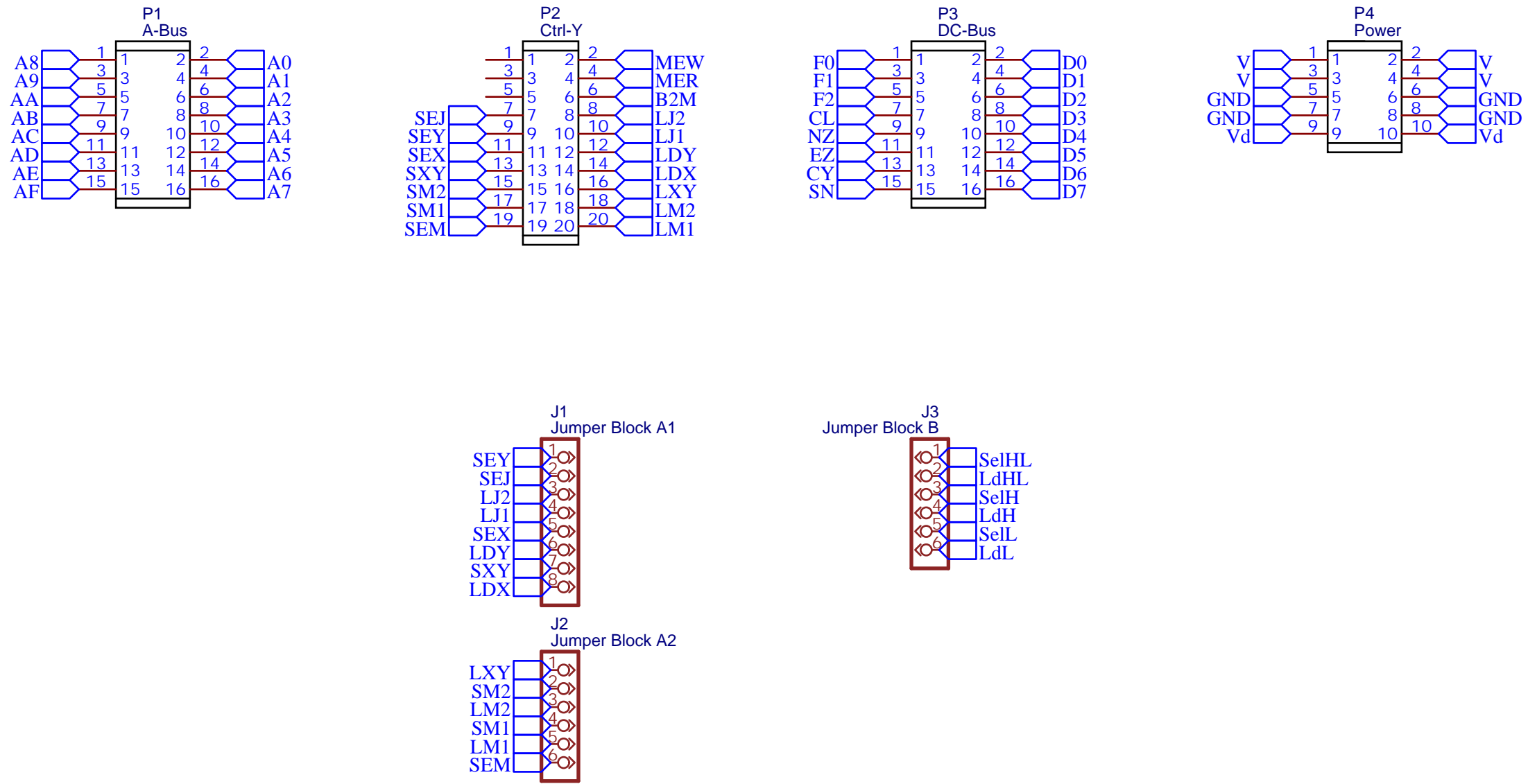


LdH, LdL and LdHL signals connect to control Y bus (sheet 4)
 SelH, SelL and SelHL signals connect to control Y bus (sheet 4)

EnH, ExL and EnHL signals connect to gating relays (sheet 2)
 HoldHL connects only on this sheet
 HoldH and HoldL signals connect to register relays (sheet 1)

TITLE: Relay Computer : Y Backplane Registers		REV: 1.0
EasyEDA	Company: Paul Law	Sheet: 3/4
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Sheet 4: Backplane connections



Jumper block A and B is used to map control signals from backplane Ctrl-Y bus

A0-AF signals connect to gating relays (sheet 2)

D0-D7 signals connect to gating relays (sheet 2)

LdH, LdL and LdHL signals connect to control relays (sheet 3)

SelH, SelL and SelHL signals connect to control relays (sheet 3)

TITLE: Relay Computer : Y Backplane Registers		REV: 1.0
EasyEDA	Company: Paul Law	Sheet: 4/4
	Date: 2019-02-10	Drawn By: paul_6392