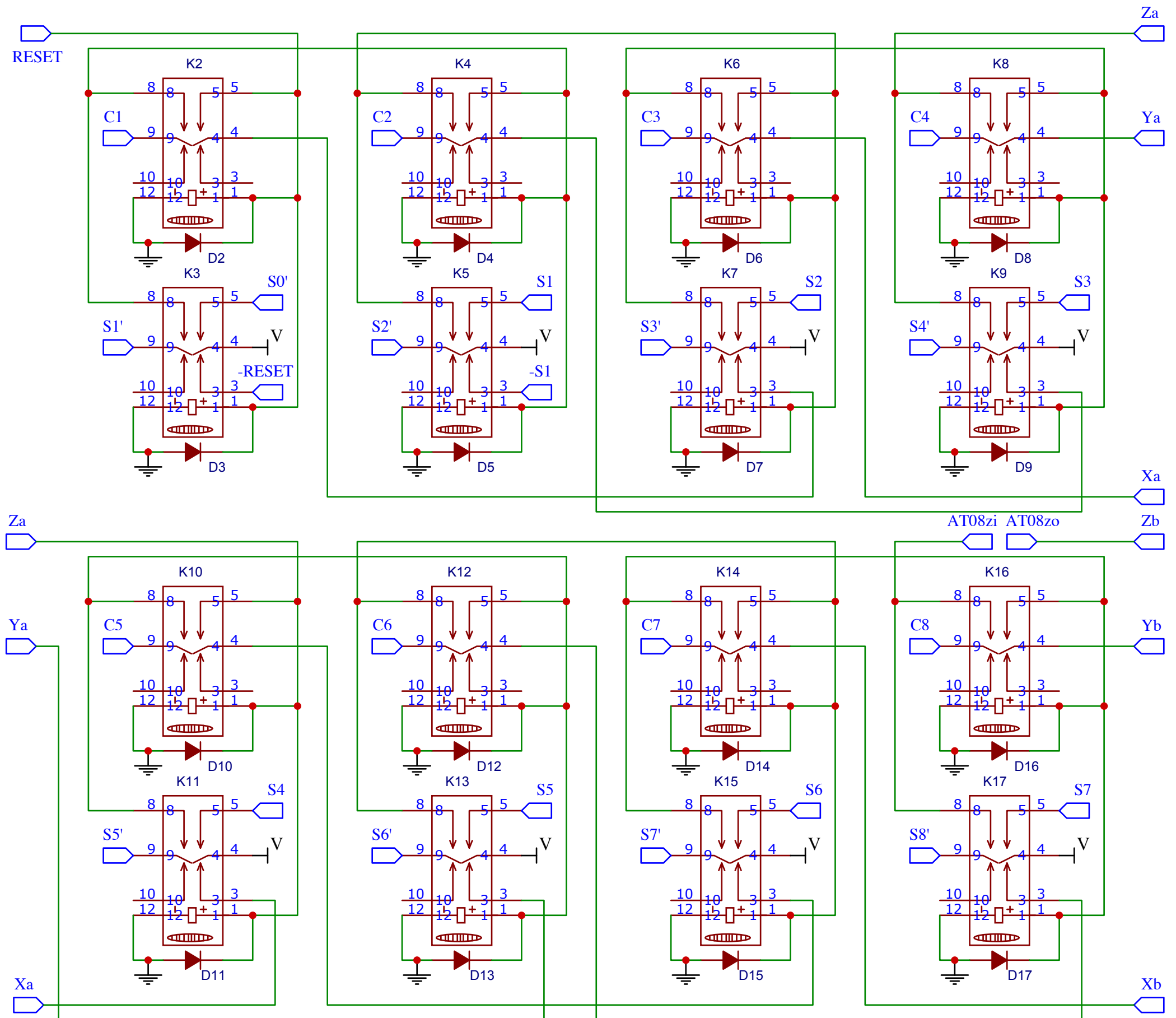
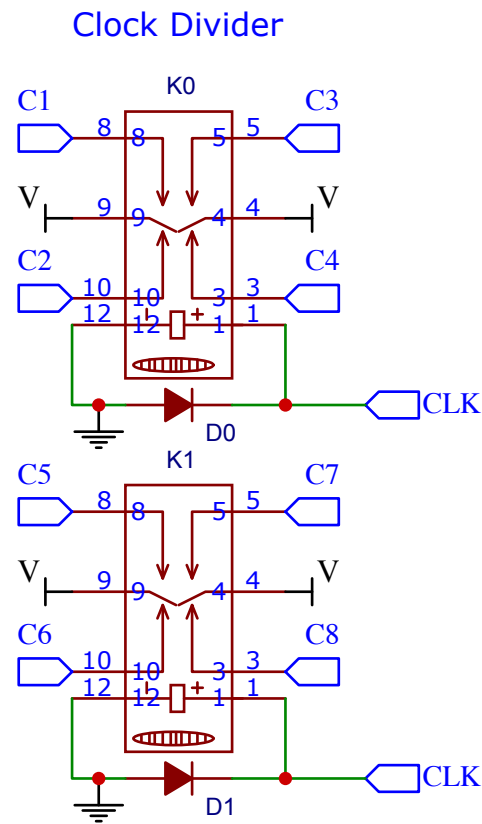


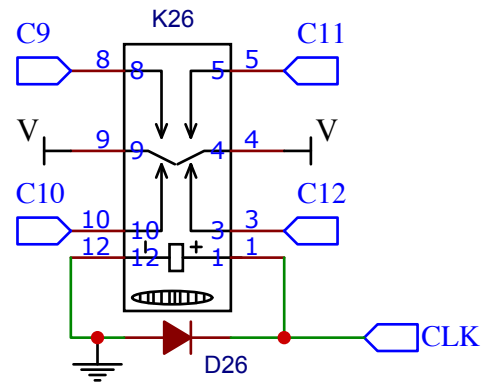
Sheet 1: 8 Stage FSM



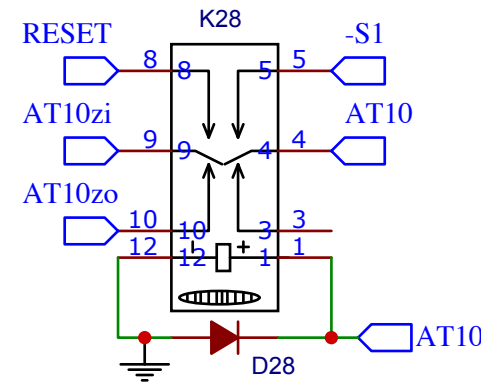
CLK and RESET signals connect to control X bus (sheet 4)  
 AT08 signal connect to OP bus via upper card interconnect (sheet 4)  
 Xb, Yb, Zb connect to next FSM stage (sheet 2)  
 S1-S7, S0'-S8', ~S1 signals connect to next FSM stage, pulse distribution and indicators (sheet 2, 3 & 5)

TITLE: Relay Computer : Sequencer Lower Card		REV: 1.0
EasyEDA	Company: Paul Law	Sheet: 1/5
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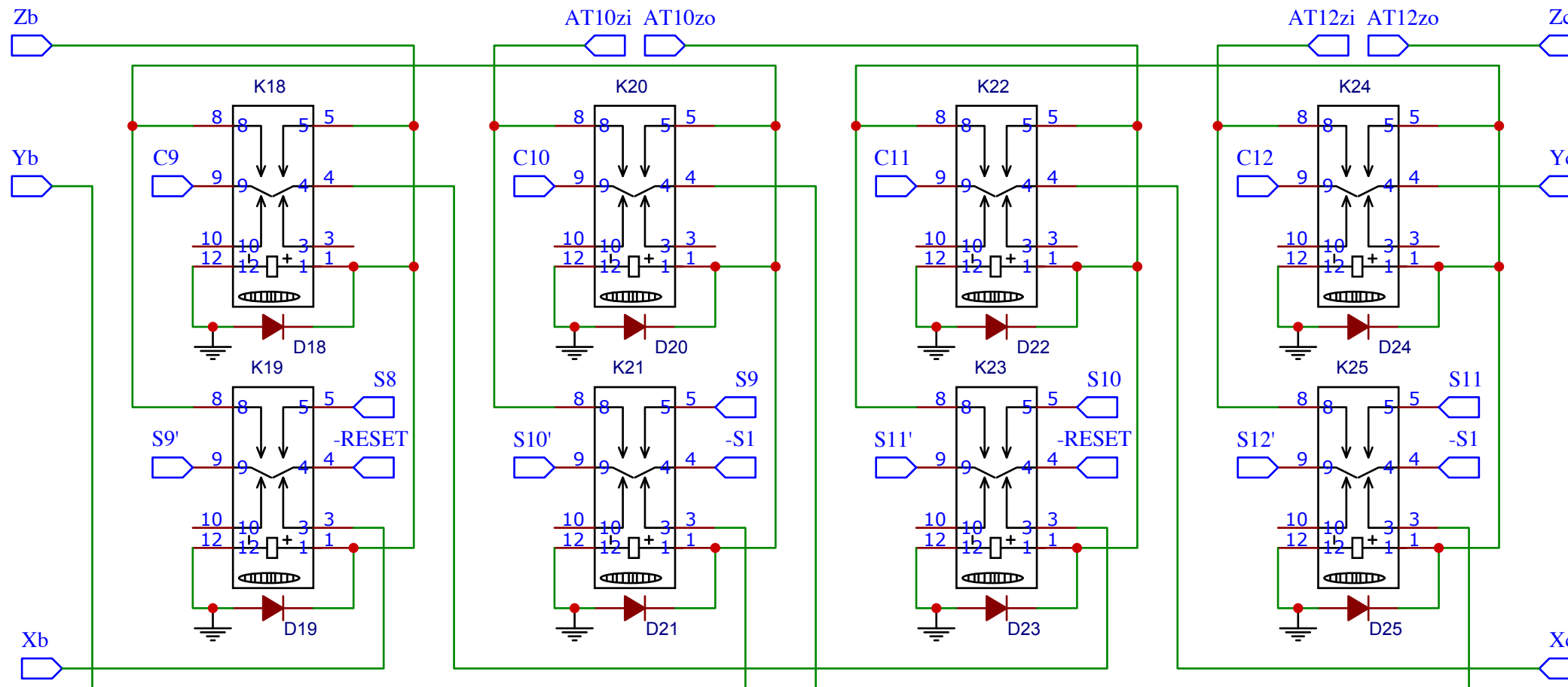
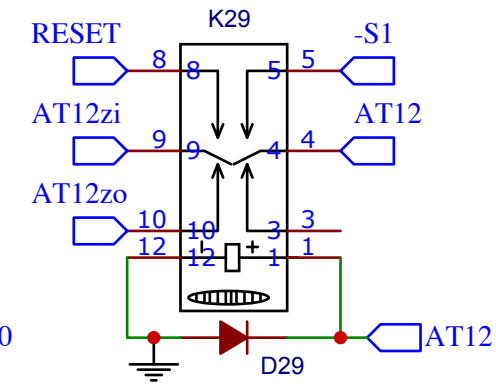
Clock Divider



Abort Latch 10



Abort Latch 12



CLK and RESET signals connect to control X bus (sheet 4)

AT10 and AT12 signal connect to OP bus via upper card interconnect (sheet 4)

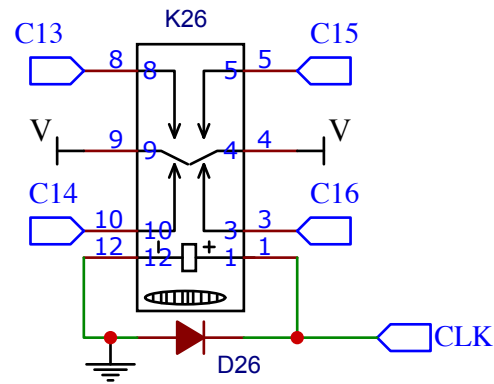
Xb, Yb, Zb connect from previous FSM stage (sheet 1)

Xc, Yc, Zc connect to next FSM stage via upper card interconnect (sheet 4)

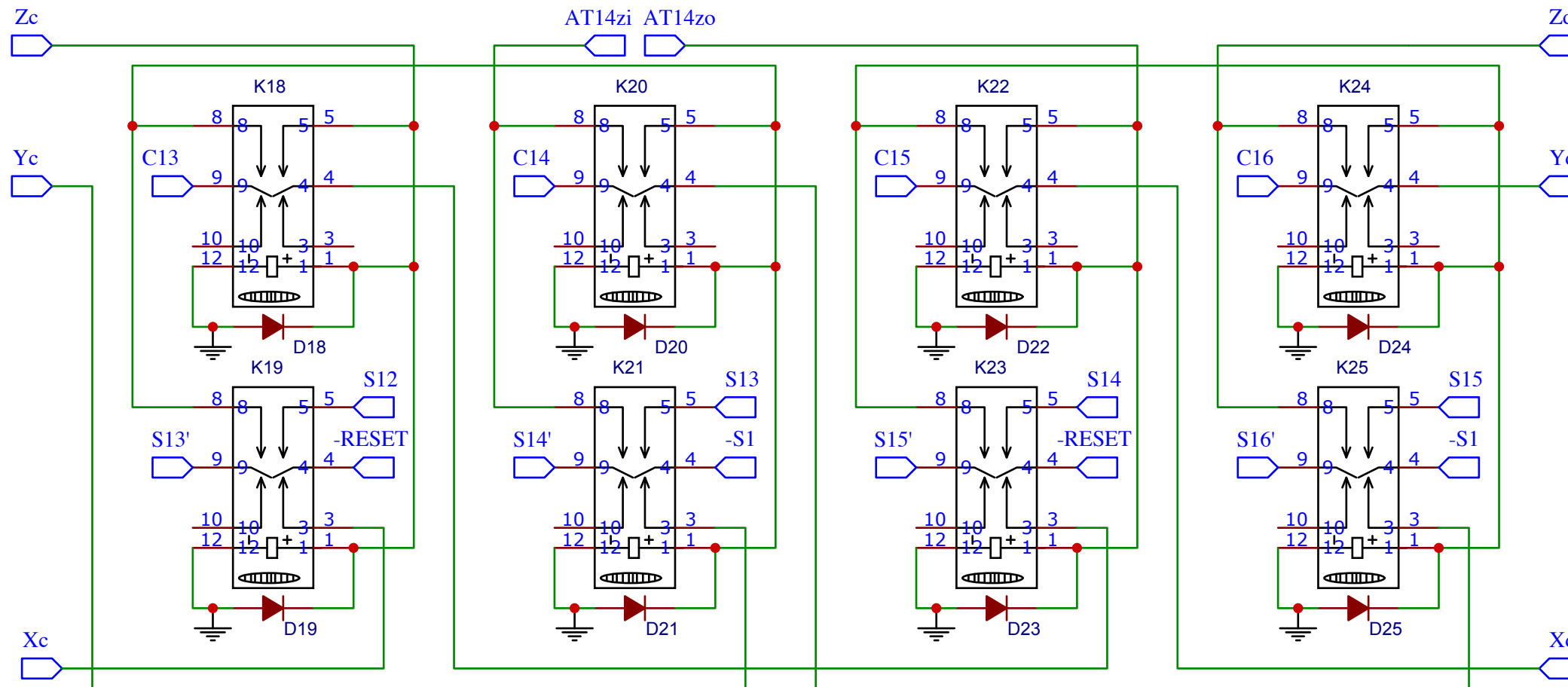
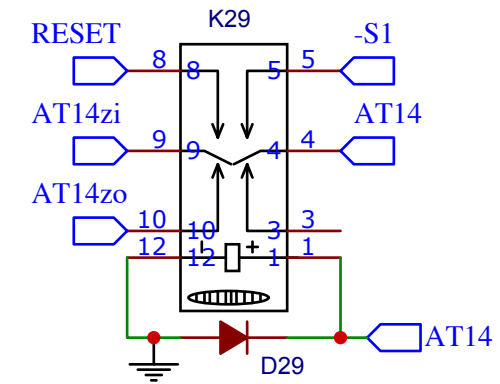
S8-S11, S9'-S12', ~S1 signals connect to prev FSM stage, pulse distribution and indicators (sheet 1, 3 & 5)

TITLE: Relay Computer : Sequencer Lower Card		REV: 1.0
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	Date: 2019-09-23	Drawn By: paul_6392

Clock Divider

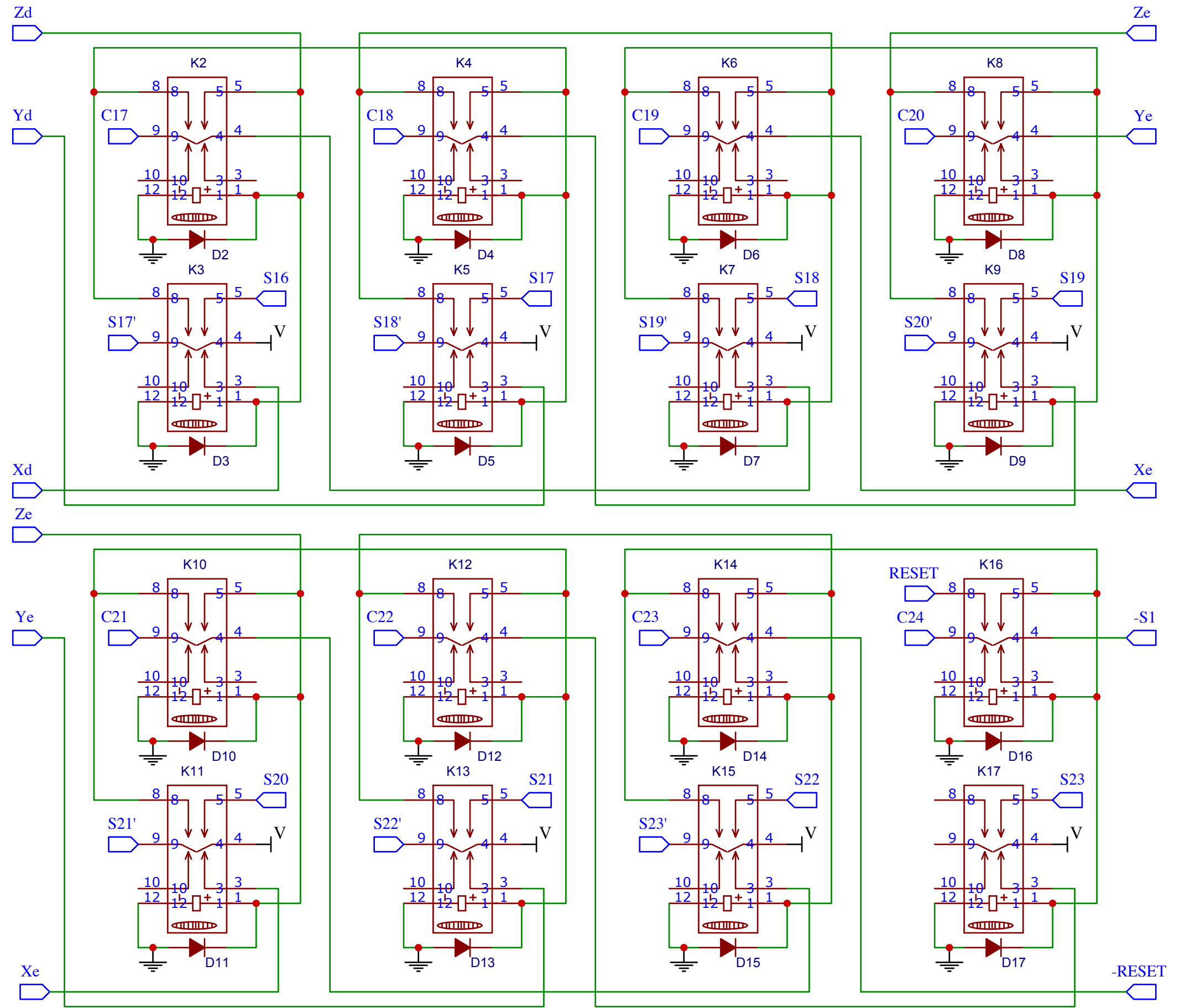
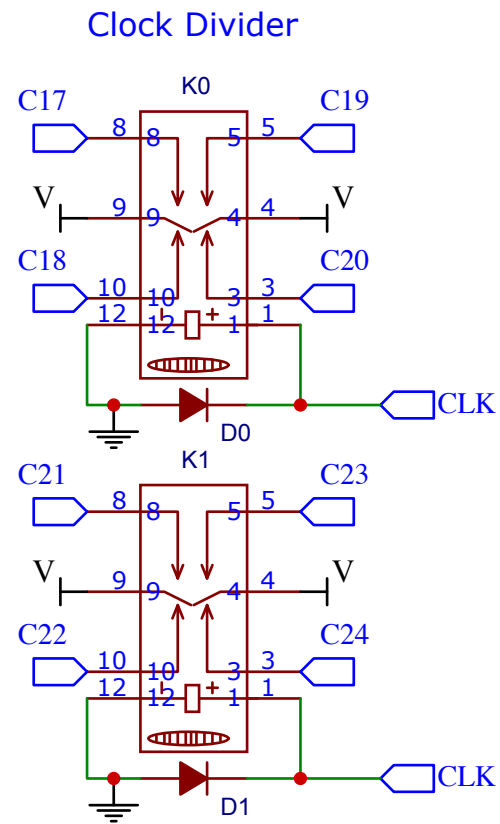


Abort Latch 14



CLK and RESET signals connect to control X bus via lower card connect (sheet 4)  
 AT14 signal connects to OP bus (sheet 4)  
 Xc, Yc, Zc connect from previous FSM stage via lower card connect (sheet 4)  
 Xd, Yd, Zd connect to next FSM stage (sheet 1)  
 S12-S15, S13'-S16', ~S1 signals connect to prev FSM stage, pulse dist and indicators (sheet 1, 3 & 5)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.0
EasyEDA	Company: Paul Law	Sheet: 2/5
	Date: 2019-09-23	Drawn By: paul_6392



CLK and RESET signals connect to control X bus via lower card connect (sheet 4)  
 Xd, Yd, Zd connect from previous FSM stage (sheet 2)  
 S16-S23, S17'-S23', ~S1 signals connect to pulse distribution and indicators (sheet 3 & 5)

TITLE: Relay Computer : Sequencer Upper Card		REV: 1.0
EasyEDA	Company: Paul Law	Sheet: 1/5
	Date: 2019-09-23	Drawn By: paul_6392